Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claim in the application:

Listing of Claims:

1. (Currently amended) A semiconductor device ~~including~~ comprising a processor having reprogrammable instructions implemented in field-programmable logic, wherein all I/O connections for ~~said~~ the field-programmable logic ~~connect~~ couple to ~~said~~the ~~DSP~~ processor.

2. (Currently Amended) A family of two or more ASIC devices ~~including~~ comprising a processor having mask-programmable instructions implemented in ASIC logic, wherein each device member of ~~said~~ the family ~~having~~ has different amounts of ASIC logic available, and wherein each member of ~~said~~ the device family ~~having~~ has substantially identical processors, processor memory, and numbers of input/output connections (I/O).

3. (Currently Amended) The ASIC device family ~~of ASIC devices~~ of claim 2, wherein all device members of ~~said~~ the family ~~can~~ are configured to plug into the same socket in a target system and function properly.

4. (Withdrawn) A method for implementing DSP software functionality in a device containing a processor and field-programmable logic, comprising: performance-profiling the execution of said DSP software functionality to identify the subroutine that dominates the overall execution time; and automatically converting, by computer means, the subroutine that dominates the overall execution time into field programmable logic functionality, such that the field programmable logic implementation of said subroutine is implemented in synchronous logic.

5. (Withdrawn) The method of claim 4 where said the field programmable logic implementation of said subroutine is implemented in logic that is synchronous with the clocks of said DSP processor.

6. (Withdrawn) The method of claim 4 where said dominant subroutine is implemented in mask-programmed ASIC logic.

7. (Withdrawn) A method for implementing DSP software functionality in a prototype device containing a processor and field-programmable logic and a production device containing mask-programmed ASIC logic functionality, comprising: performance-profiling the execution of said DSP software functionality to identify the subroutine that dominates the overall execution time; and converting the subroutine that dominates the overall execution time into field-programmable logic functionality; and evaluating the device size and speed required for implementation in a production device where the function implemented in said field-programmable logic functionality is instead implemented using mask-programmed ASIC logic functionality.

8. (New) The semiconductor device of claim 1, wherein the processor comprises a DSP processor.

9. (New) An integrated circuit, comprising:

a fixed portion comprising one or more fixed logic blocks;

a reprogrammable portion comprising a plurality of reprogrammable logic blocks; and

instruction logic coupled to the one or more fixed logic blocks and to the plurality of reprogrammable logic blocks, wherein the instruction logic is configured to decode an instruction stream of a software program to sequentially provide control signals to the one or more fixed logic blocks and to the plurality of reprogrammable logic blocks according to a sequence of execution of the software program.

10. (New) The integrated circuit of claim 9, wherein the instruction logic is further configured to wait until the reprogrammable portion returns a result from an operation performed according to an instruction of the software program before providing an immediately subsequent instruction of the software program to the fixed portion.

11. (New) The integrated circuit of claim 9, wherein the reprogrammable portion is subordinate to the fixed portion.

12. (New) The integrated circuit of claim 9, wherein the fixed portion is a software-programmable digital signal processor (DSP).

13. (New) The integrated circuit of claim 9, wherein the reprogrammable portion is a field-programmable gate array (FPGA).

14. (New) The integrated circuit of claim 9, wherein substantially all of the plurality of reprogrammable logic blocks are identical.

15. (New) The integrated circuit of claim 9, wherein the plurality of reprogrammable logic blocks include at least two different reprogrammable logic block types that differs by an amount of logic and/or a type of logic.

16. (New) The integrated circuit of claim 9, wherein the reprogrammable portion further comprises at least one application-specific function block.

17. (New) The integrated circuit of claim 16, wherein the at least one application-specific function block is a Multiplier, Barrel Shifter, Bit-Reverse Address Generator, Auto-Scaling Unit, Large Multiplier, or Viterbi Decoder.

18. (New) The integrated circuit of claim 9, wherein the fixed portion comprises the instruction logic.

19. (New) The integrated circuit of claim 9, wherein the instruction logic is at least partially reprogrammable to provide a reprogrammable instruction set.

20. (New) The integrated circuit of claim 19, wherein the at least partially reprogrammable instruction logic is configured to perform instruction decoding for at least some of the fixed portion.

21. (New) The integrated circuit of claim 19, wherein the at least partially reprogrammable instruction logic comprises:

a content-addressable memory (CAM) configured to accept results signals from the fixed function blocks, the reprogrammable logic blocks, and/or data path elements of the integrated circuit, and to encode the accepted results signals; and

a memory element comprising:

a first set of address inputs, coupled to outputs of the CAM, to receive an encoded signal from the CAM; and

a second set of address inputs, coupled to an instruction fetch logic element of the integrated circuit, to accept instruction signals according to the software program, and to decode the encoded signal to control the plurality of reprogrammable logic blocks and/or the one or more fixed logic blocks.